NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD) 96-06-26	Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME *(First, Middle Initial, Last)*

b. ADDRESS *(Street, City, State, Zip Code)*
Defense Electronics Supply Center
1507 Wilmington Pike
Dayton, OH 45444-5765

5. CAGE CODE 67268

6. NOR NO. 5962-R156-96

7. CAGE CODE 67268

8. DOCUMENT NO. **86023**

9. TITLE OF DOCUMENT

MICROCIRCUIT, DIGITAL, BIPOLAR 256-BIT RAM, MONOLITHIC SILICON

10. REVISION LETTER

a. CURRENT A	b. NEW B

11. ECP NO.

N/A

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

```
Sheet 1:  Revisions ltr column; delete "A" and add "B".
          Revisions description column; add "Changes in accordance with NOR 5962-R156-96".
          Revisions date column; add "96-06-26".
          Rev status above sheet numbers 1, delete "A" and add "B".
          Revision level block; delete "A" and Add "B".

          On sheet 1 in the open area between the Revision information and above the first row of REV
          blocks; write in bold lettering the following: "CURRENT CAGE CODE 67268".
```

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*

X	(1) Existing document supplemented by the NOR may be used in manufacture.
	(2) Revised document must be received before manufacturer may incorporate this change.
	(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT

DESC-ELDS

c. TYPED NAME *(First, Middle Initial, Last)*

Michael A. Frye

d. TITLE

Microelectronics Branch Chief

e. SIGNATURE

Michael A. Frye

f. DATE SIGNED *(YYMMDD)* 96-06-26

15a. ACTIVITY ACCOMPLISHING REVISION

DESC-ELDS

b. REVISION COMPLETED *(Signature)*

Kenneth S. Rice

c. DATE SIGNED *(YYMMDD)* 96-06-26

DD Form 1695, APR 92   *Previous editions are obsolete.*
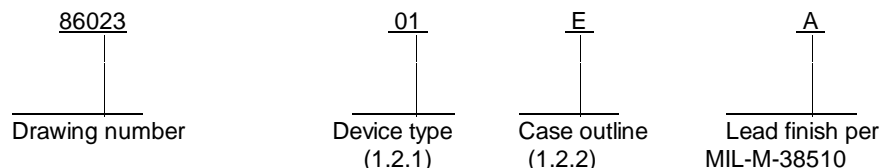
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change supply voltage. Change junction temperature. Change to military drawing format.	14 April 1987	N A Hauck

REV																		
SHEET																		
REV																		
SHEET																		

REV STATUS OF SHEETS			REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
			SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Defense Electronics Supply Center Dayton, Ohio **Original date of drawing**: 3 March 1986 **AMSC N/A**	PREPARED BY Rick C. Officer	**MILITARY DRAWING** **This drawing is available for use by all Departments and Agencies of the Department of Defense**
	CHECKED BY D A Di Cenzo	
	APPROVED BY N A Hauck	TITLE: MICROCIRCUITS, DIGITAL, BIPOLAR 256-BIT RAM, MONOLITHIC SILICON
	SIZE **A** / CODE IDENT. NO. **14933**	DWG NO. **86023**
	REVISION LEVEL A	SHEET 1 OF 14

5962-E345

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MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883 "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

```
    86023              01          E            A
      |                 |          |            |
      |                 |          |            |
Drawing number    Device type  Case outline  Lead finish per
                   (1.2.1)      (1.2.2)      MIL-M-38510
```

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit
01	82S16	256-bit X 1 bipolar RAM

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16 lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16 lead, 1/4" x 3/8"), flat package

1.3 Absolute maximum ratings.
Supply voltage . . . . +7 V dc maximum
Output voltage . . . . +5.5 V dc maximum
Storage temperature range . . . . -65°C to +150°C
Maximum power dissipation (P_D) 1/ . . . . 660 mW
Lead temperature (soldering, 10 seconds) . . . . +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Cases E and F . . . . See MIL-M-38510, appendix C
Junction temperature (T_J . . . . +200°C

1.4 Recommended operating conditions.
Supply voltage . . . . +4.75 V dc to +5.25 V dc
Case operating temperature range (T_C) . . . . -55°C to +125°C
Maximum high level input voltage . . . . +2.0 V dc
Maximum low level input voltage . . . . +0.8 V dc

_____

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

  MILITARY

   MIL-M-38510   -   Microcircuits, General Specification for.

STANDARD

  MILITARY

   MIL-STD-883   -   Test Methods and Procedures for Microelectronics.

  (Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	1/ Conditions $-55°C \leq T_C \leq +125°C$ $4.75\ V \leq V_{CC} \leq 5.25\ V$ see figure 4		Group A subgroups	Limits Min	Limits Max	Unit
High-level input voltage	V_{IH}	V_{CC} = maximum		1, 2, 3	2.0		V
Low-level input voltage	V_{IL}	V_{CC} = minimum		1, 2, 3		0.8	V
Clamp voltage	V_{IC}	V_{CC} = minimum, I_{IN} = -18 mA		1, 2, 3		-1.5	V
High-level output voltage 2/	V_{OH}	V_{CC} = minimum, I_{OH} = -3.2 mA		1, 2, 3	2.4		V
Low-level output voltage 3/	V_{OL}	V_{CC} = minimum, I_{OL} = 16 mA		1, 2, 3		0.5	V
High-level input current 4/	I_{IH}	V_{CC} = maximum, V_{IN} = 5.5 V		1, 2, 3		25	µA
Low-level input current 4/	I_{IL}	V_{CC} = maximum, V_{IN} = 0.45 V		1, 2, 3		-250	µA
Hi-Z state output current 5/	I_{OZ}	V_{CC} = maximum	V_{OUT} = 5.5 V	1, 2, 3		50	µA
			V_{OUT} = 0.45 V			-50	
Short circuit current 6/	I_{OS}	V_{CC} = maximum,	V_O = 0 V	1, 2, 3	-15	-70	mA
V_{CC} supply current 7/	I_{CC}	V_{CC} = maximum, CE_1, or CE_2, or CE_3 = high		1, 2, 3		120	mA
Address access time	T_{AA}	$4.75\ V \leq V_{CC} \leq 5.25\ V$ See figure 5		9, 10, 11		70	ns
Chip enable access time	T_{CE}	$4.75\ V \leq V_{CC} \leq 5.25\ V$		9, 10, 11		40	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	1/ Conditions -55° C ≤ T_C ≤ +125° C 4.75 V ≤ V_{CC} ≤ 5.25 V see figure 4	Group A subgroups	Limits Min	Limits Max	Unit
Disable time	T_{CD}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11		40	ns
Valid time	T_{WD}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11		55	ns
Address setup time	T_{WSA}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	20		ns
Address hold time	T_{WHA}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	10		ns
Data in setup time	T_{WSD}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	50		ns
Data in hold time	T_{WHD}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	10		ns
CE setup time	T_{WSC}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	10		ns
CE hold time	T_{WHC}	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	10		ns
Write enable pulse width	T_{WP} 8/	4.75 V ≤ V_{CC} ≤ 5.25 V	9, 10, 11	40		ns

1/ All voltage values with respect to ground.
2/ Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
3/ Measured with a logic low stored and V_{IL} applied to CE_1, CE_2, and CE_3.
4/ Test each input one at a time.
5/ Measured with V_{IH} applied to CE_1, CE_2, and CE_3.
6/ Duration of the short circuit should not exceed 1 second.
7/ I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at
    4.5 V and the output open.
8/ Minimum required to guarantee a write into the slowest bit.

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3.6 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 <u>Notification of change</u>. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1)   Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125° C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 <u>Group A inspection</u>.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 <u>Groups C and D inspections</u>.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1)   Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125° C, minimum.

(3)   Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

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CASES E AND F

```
           ┌────┐ ┌────┐
       A1 ─┤ 1        16 ├─ V_CC
       A0 ─┤ 2        15 ├─ A2
      CE1 ─┤ 3        14 ├─ A3
      CE2 ─┤ 4        13 ├─ D_IN
      CE3 ─┤ 5        12 ├─ WE
     D_OUT ─┤ 6        11 ├─ A7
       A4 ─┤ 7        10 ├─ A6
      GND ─┤ 8         9 ├─ A5
           └──────────────┘
```
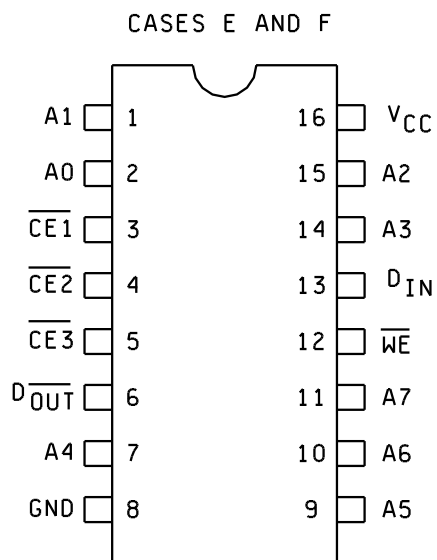
FIGURE 1. Terminal connections.

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MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored data
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

* "0" = All $\overline{CE}$ inputs low;
"1" = One or more $\overline{CE}$ inputs high.
 X = Don't care.

FIGURE 2. Truth table.

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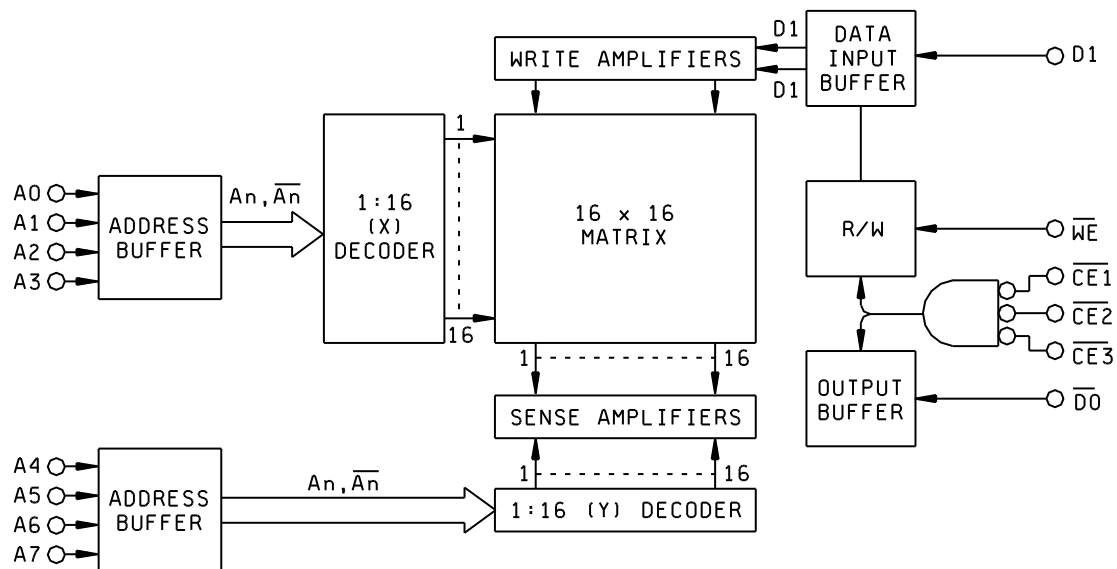
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FIGURE 3. Logic diagram.

INPUT PULSES

ALL INPUT PULSES

```
+3.0 V ─────────┐               ┌── 90%
                 \             /
  0 V ───────────┘            └──┼── 10%
        ≤ 5 ns ──┤├─        ─┤├── ≤ 5 ns
```

```
+3.0 V ─────────┐               ┌──
                 \             /  10%
  0 V ───────────┘    90%    └──
        ≤ 5 ns ──┤├─        ─┤├── ≤ 5 ns
```

MEASUREMENTS ALL CIRCUIT DELAYS ARE MEASURED
AT THE +15 LEVEL OF INPUTS AND OUTPUTS

LOADING CONDITION

V_CC
1 k

PULSE
GENERATOR

1 k
+5.0 V

PULSE
GENERATOR

PULSE
GENERATOR

V_CC

A0 A1 A2 A3   V_CC
A4
A5
A6
A7

DUT

WE

D_IN

CE1,2,3

GND

V_CC
R_1
DO
R_2   C_L
           CAPACITANCE INCLUDING
           SCOPE AND JIG

FIGURE 4. Test load circuit and voltage waveform.

READ CYCLE

ADDRESS   1.5 V   +3.0 V
                                                    0 V

                        "0" STORED
                                                    V_OH
DO   1.5 V   "1" STORED
                                                    V_OL

        |← t_AA →|

ADDRESS ACCESS TIME

$\overline{CE}$ 1.5 V   +3.0 V

        |← t_CE →| t_CD

$\overline{D}_O$ HI-Z   1.5 V   "1" LEVEL   0.5 V
                                             0.5 V   HI-Z
                           "0" LEVEL
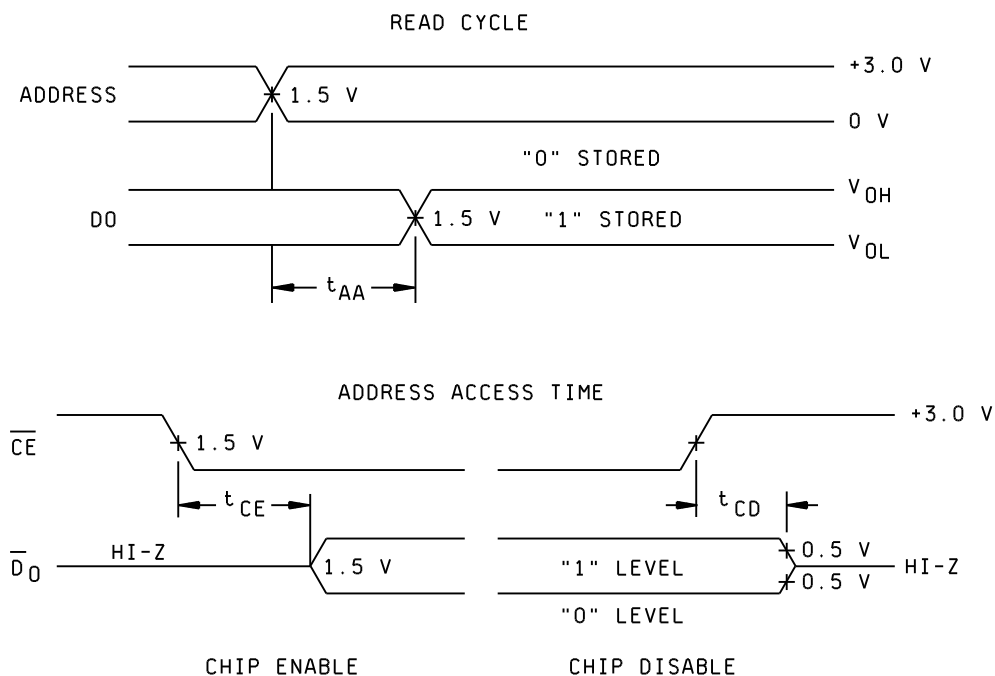
        CHIP ENABLE   CHIP DISABLE

FIGURE 5. Timing diagrams.

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WRITE CYCLE
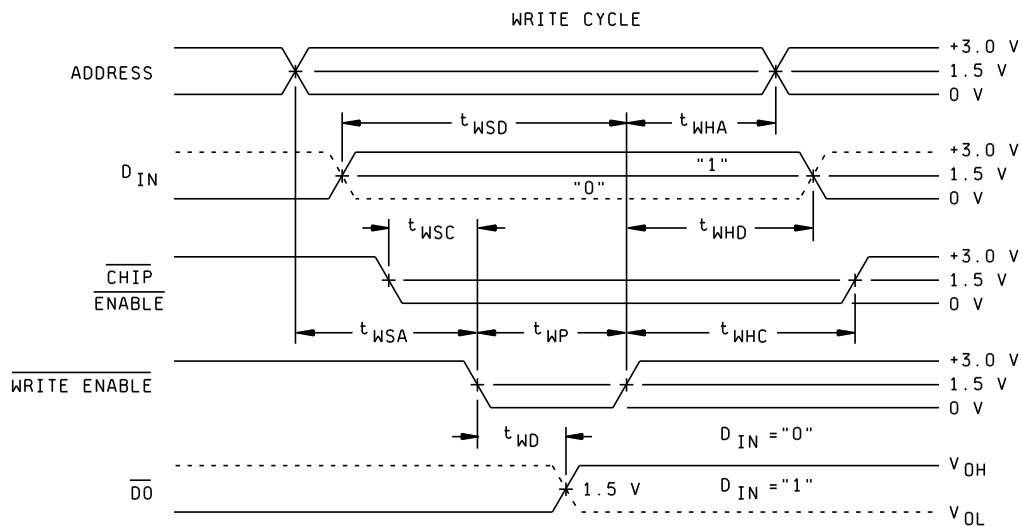
MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of chip enable low (with address valid) and when data output becomes valid

T_{CD} Delay between when chip enable becomes high and data output is in off state.

T_{AA} Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

T_{WSC} Required delay between beginning of valid chip enable and beginning of write enable pulse.

T_{WHD} Required delay between end of write enable pulse and end of valid input data.

T_{WP} Write of write enable pulse.

T_{WSA} Required delay between beginning of valid address and beginning of write enable pulse.

T_{WSD} Required delay between beginning of valid data input and end of write enable pulse.

T_{WD} Delay between beginning of write enable pulse and when data output reflects complement of data input.

W_{WHC} Required delay between end of write enable pulse and end of chip enable.

T_{WHA} Required delay between end of write enable pulse and end of valid address.

FIGURE 5. Timing diagrams - Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
8602301EX	18324	82S16/BEA	---
8602301FX	18324	82S16/BFA	---

1/ Caution. Do not use this number for item acquisition. Items acquired to
     this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics, Incorporated 4130 S. Market Court Sacramento, CA 95834

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